IN THE CLAIMS

1. (Currently Amended) A method for processing a memory access request within processing architecture, comprising the steps of: determining whether the memory access request is speculative or not based upon a first identifier; assessing one or both of interconnect and target resource conditions in the event that the memory access request is speculative; and either processing the memory access request, or not, as a function of the conditions.

2. (Currently Amended) The method of claim 1, wherein the step of determining whether the memory access request is speculative comprises decoding the first identifier as a first bit field within the memory access request.

3. (Currently Amended) The method of claim 2, further comprising encoding the first bit field within the memory access request to define a speculative ID of the memory access request.

4. (Currently Amended) The method of claim 1, wherein the memory access request comprises one of an instruction, a message and an operational request.

5. (Currently Amended) The method of claim 1, further comprising the step of determining a priority of the memory access request based upon a second identifier, in the event that the memory access request is speculative, and wherein the step of processing the memory access request comprises processing the memory access request, or not, based upon the conditions and the priority.

6. (Currently Amended) The method of claim 5, wherein the step of determining a priority comprises decoding the second identifier as a second bit field within the memory access request.

7. (Currently Amended) The method of claim 6, further comprising encoding the second bit field within the memory access request to define a priority of the memory access request.

8. (Currently Amended) The method of claim 1, wherein the memory access request comprises one of a memory read request and a memory load request.

9. (Currently Amended) The method of claim 1, wherein the step of determining comprises utilizing one of a CPU, chipset and memory controller to determine whether the memory access request is speculative.

10. (Currently Amended) The method of claim 9, wherein at least one of the CPU, chipset and memory controller independently controls the step of processing the memory access request based on the conditions.

11. (Original) The method of claim 1, wherein the step of assessing target resource conditions comprises assessing one or more of memory utilization, memory congestion, buffer space utilization, and bus congestion.

12. (Original) The method of claim 1, wherein the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization.

13. (Currently Amended) The method of claim 1, further comprising the step of notifying one or more logic devices when the memory access request is not processed.

14. (Currently Amended) In CPU architecture ~~of the type~~ that initiates both speculative and non-speculative memory access requests, ~~the~~ an improvement comprising decode logic for determining whether the memory access requests are speculative, and assessment logic for determining one or both of interconnect and target resource conditions, the CPU architecture processing speculative memory access requests, or not, as a function of the conditions.

15. (Currently Amended) In CPU architecture of claim 14, the further improvement comprising a prefetch unit for prefetching speculative memory access requests, wherein the decode logic detects whether prefetched memory access requests are speculative.

16. (Currently Amended) A system for processing speculative memory access requests within a processing architecture, comprising: one or more memory access requests having a bit field defining the memory access requests as speculative or non-speculative; decode logic for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic for processing speculative memory access requests, or not, based on at least one of interconnect and target resource conditions.

17. (Currently Amended) A system of claim 16, one or both of the decode logic and processing logic being ~~selected from~~ located within one of ~~the group consisting essentially of~~ a CPU, a chipset, a bus controller ~~and~~ or a memory controller.

18. (Currently Amended) A system of claim 16, wherein the memory access requests comprise memory read instructions.

19. (Original) A system of claim 16, further comprising a bus controller for assessing one or more of bus congestion and bus utilization conditions.